REMARKS

The Applicants thank the Examiner for the telephone interview on June 4, 2003.

Claims 1, 2,8-10 and 16-22 are pending in the application. Claims 18 – 22 have been canceled without prejudice. Claims 1, 2, 16 and 17 have been allowed. Amendments have been made to claims 1, 8,and 16 for clarification purposes. New claims 23 – 25 have been added. Amendments also have been made to the specification and the drawings to correct certain informalities for clarification purposes. No new matter has been included thereby.

In the specification

In Fig. 3d, drain region 59 was inadvertently referred to as 58. The first paragraph on page 8 has been amended to refer to drain 59.

In the drawings

In Fig. 3d, drain region 59 was inadvertently mislabeled 58. It has been corrected to 59. A marked up sheet for sheet #2, which includes the proposed changes to Fig. 3d, is submitted as part of this amendment for the Examiner's review.

Allowable Subject Matter

In the Office Action mailed March 14, 2003, the Examiner allowed claims 1, 2, 16 and 17.

Claim Rejection under 102

The Examiner rejected claims 8-9 as being anticipated by Eitan et al. (US Patent No. 4,998,220). Applicants respectfully disagree.

In particular, Eitan et al. failed to show or suggest the claimed combination of elements for a flash memory array recited in claim 8. Claim 8 recites, among other

things, a memory array disposed on a substrate comprising a plurality of memory cells each having a channel region formed in the substrate, a floating gate separated from said channel region by a first insulating layer, an erase gate, a control gate separated from the floating gate by a second insulating layer, a source region, and a drain region.

The Examiner indicated that Eitan suggested a substrate (103) having a channel region (107a) (see Figs. 5 and 7a and abstract). The Applicants respectfully point out that 107a is not a channel region; rather it is a "channel stop" region, more heavily doped to prevent a channel from forming. It is stated in Eitan et al. Col. 8, lines 17 – 23, that " Region 107a is more heavily doped with P type impurities than P – substrate 103 to form a channel stop under portion 104a' of floating gate 104a. Oxide 105a and region 107a prevent a conductive channel from forming between source 110 and drain 102a under portion 104a' of floating gate 104a,"

There are many other differences between Eitan and the Applicants' invention. For example, the Examiner indicated that Eitan included "a first insulating layer (portion of layer 105a which is between the floating gat 104a and the channel region 107a)". As pointed out earlier, 107a is not a channel region and oxide 105a is a field oxide approximately 6000 A thick. Further Eitan et al. stated in col. 5 lines 41 – 45 "An array of floating gates is formed such that each floating gate includes a first portion extending between a pair of associated source/drain regions and a second portion extending over the field oxide." Eitan et al. also described in col. 5 lines 47 – 50, "An erase gate extends over the field oxide and the second portion of the floating gates ..."

Therefore, Eitan et al. described a different device than the Applicants' invention as recited in claim 8, which also includes a plurality of rows and columns of interconnected memory cells with the control gates of memory cells in the same row are connected by a common word-line, the erase gates of the memory cells in the same row are connected by a common erase line, the source regions of the memory cells in the

same rows are connected by a common source line, and the drain regions of memory cells in the same columns are commonly connected via a common drain line

The invention of claim 8 further includes that at least a portion of each control gate is disposed over a portion of the channel region and is separated therefrom by the second insulating layer, and wherein a portion of the control gate is disposed in facing relationship to a side surface of the floating gate and is separated therefrom by the second insulating layer; and a control circuit connecting to the word-lines, erase lines, source lines and drain lines for operating one or more memory cells of the memory array

In summary, Eitan et al. fails to show or suggest the combination of elements of the instant invention as recited in claim 8. Accordingly, claim 8 is patentable over Eitan et al.

Dependent claim 9 that is dependant from claim 8 is at least patentable for the reasons given above. Here, Eitan et al. does not show or suggest the combination of elements included in claim 9 when combined with independent claim 8.

Claim Rejection under 103

The Examiner rejected claim 10 as being unpatentable over Eitan et al. (US Patent No. 4,998,220) in view of Chang (US Patent No. 6,125,060). Because claim 10 depends from claim 9, claim10 is therefore patentable for at least the reasons given above

New Claims

New claims 23 – 25 have been added, which are similar to claims 8 – 10, but included the limitation that the channel region under the control gate and uncovered by the floating gate is proximate to the drain region to further differentiate from the prior art. In Eitan, Figs 8c and 9c the floating gate 104a is used to form self-aligned drain 102a and 102a', (see Eitan col. 11, lines 14 – 19) therefore the channel region under the control

gate and uncovered by the floating gate is proximate to the source region 110. This can also be seen in Figs. 5, 5a, 5b, 5c, and Fig. 6, etc.

Having thus amended the application for clarification and having established that the cited references, either taken either singly or collectively, failed to show or suggest the combination of claim elements of the claims in the present application, Applicants respectfully submit that claims 8 – 10 of the application are in condition for allowance. It is respectfully requested that rejection of claims 8 - 10 be reconsidered, and early notice thereof is solicited for the allowability for claims 8 – 10 as currently amended, as well as for claims 1,2, 16 and 17 which the Examiner allowed in the March 14, 2002 Office Action.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 408-474-1634.

Respectfully submitted,

Dah-Bin Kao

Dah-Bin Kao
Reg. No. 53,092

Winbond Electronics Corporation America
2727 North First Street
San Jose, California 95134
Tel: 408-474-1634
Fax: 408-544-1787

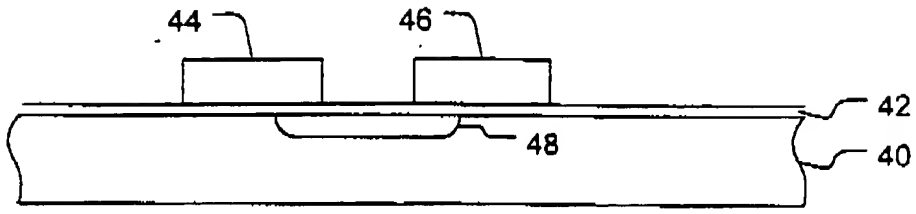

Fig. 3a

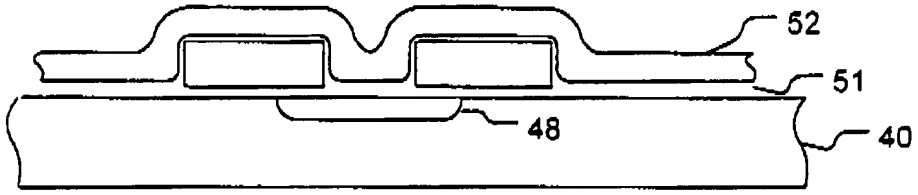

Fig. 3b

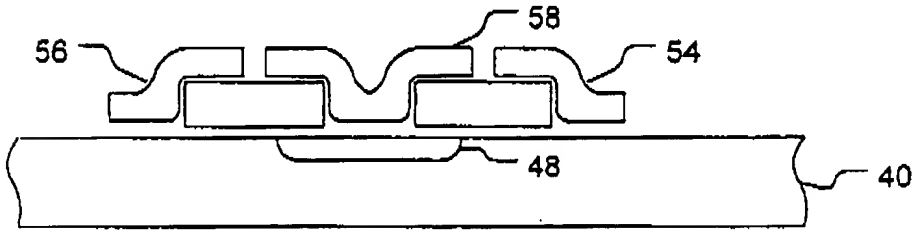

Fig. 3c

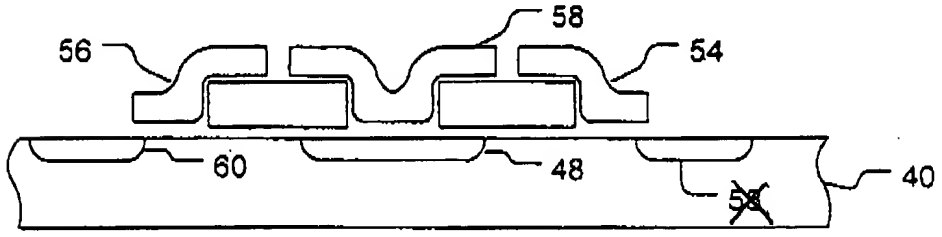

Fig. 3d